II. REMARKS

As an initial matter, Applicants note that the Examiner has not yet acknowledged Applicants' foreign priority claim. The specification has been previously amended in Preliminary Amendment (A) filed September 15, 2006, to incorporate the International and Japanese priority applications by reference. Applicants respectfully request that the Examiner acknowledge Applicants' foreign priority (i.e., Japanese priority) claim.

Applicants also note that Examiner has not indicated that the drawings filed September 15, 2006 are acceptable. Applicants respectfully requests that the Examiner accept Applicants' drawings filed September 15, 2006.

In the non-final Office Action mailed January 7, 2009, p. 5, lines 6-7, the Examiner rejects claim 3 under 35 U.S.C. § 102(b) as allegedly unpatentable over Wieczorek'696 in view of Maniar et al. (U.S. Patent No. 5,652,176, hereafter "Maniar'176"). However, Applicants note that Maniar'176 has not been listed in any documents including the Information Disclosure Statements (IDS) filed September 15, 2006 and April 23, 2009, and the Form PTO-892 attached with Office Action mailed March 10, 2009. Therefore, Applicants respectfully request that the Examiner provide Applicants with a Form PTO-892 listing Maniar'176 and a copy thereof, along with the next communication from the Office.

With the above amendment, claims 1 and 7 have been amended, claims 2 and 3 have been cancelled, and new claim 11 has been added.

Specifically, claim 1 has been amended to incorporate, one of the subject matter from previous claim 2 as cancelled, i.e., "wherein the expansion layer is made of a silicide." Claim 7 has been amended to recite "wherein the expansion flow layer fills the concave and convex portion" as supported on Fig. 7E and p. 19, line 12 to p. 20, line 4 of Applicants' disclosure as originally filed. Claims 1 and 7 have been also amended to improve grammar and clarity.

New independent claim 11 incorporates the subject matter from previous claims 1 and 3, and corresponds to previous claim 3 rewritten in independent form. Therefore, new claim 11 has the same scope as previous claim 3 as cancelled.

The present amendment adds no new matter to the above-captioned application.

A. The Invention

The present invention relates to a method for manufacturing semiconductor device including an insulating film formed on a semiconductor substrate (wafer) in which voids (bubbles) are completely eliminated.

In accordance with an embodiment of the present invention, a method for manufacturing semiconductor device is provided that includes steps recited in independent claims 1, 7 and 11.

Various other embodiments, in accordance with the present invention, are recited in dependent claims 4-6 and 8-10.

An advantage provided by various embodiments of the present invention is that a method for manufacturing semiconductor device can be provided that comprises an expansion step in which a semiconductor device can be oxidized and expanded under lower pressure (i.e., atmospheric pressure) and lower heat temperature (i.e., 400 to 800 °C) for a short period, as compared with conventional methods, thereby reducing damage due to heat treatment in further integrating the semiconductor device.

B. The Rejections

Claims 1, 2, 5-7, 9 and 10 stand rejected under 35 U.S.C. § 102(a) as allegedly anticipated over Wieczorek et al. (U.S. Patent Application Publication No. 2004/0018696, hereafter "Wieczorek'696").

Claims 2 and 8 stand rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Wieczorek'696 in combination with Ishitsuka et al. (U.S. patent No. 6,881,646, hereafter "Ishitsuka'646")

Claim 4 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Wieczorek'696 in combination with admitted prior art (JP 5-57607 and JP10-275805).

Claim 3 stands rejected under 35 U.S.C. § 103(a) as allegedly unpatentable over Wieczorek'696 in combination with Maniar'176.

Applicant respectfully traverses the Examiner's rejections and request reconsideration of the above-captioned application for the following reasons.

C. Applicant's Arguments

a. The Section 102 Rejection

Anticipation under 35 U.S.C. § 102 requires showing the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984).

In this case, the Examiner has failed to establish a prima facie case of anticipation against claims 1, 5-7 and 9-11 because Wieczorek'696 does not teach, or suggest, each and every limitation recited by these claims.

i. Wieczorek'696

Wieczorek'696 relates to a method of filling a trench formed in a substrate with an insulating material, which may be used in fabricating sophisticated integrated circuits, such as resistors, capacitors, transistors and the like. Wieczorek'696, p. 1, paragraphs [0002] to

[0003]. A semiconductor structure (200) as illustrated in Fig. 2c (see below) of Wieczorek'696, includes a substrate (201), a spacer layer (220) deposited on a trench (204) of the substrate (201), and a dielectric layer (206) formed on the spacer layer (220). Wieczorek'696, p. 3, paragraph [0032] to p. 4, paragraph [0033].

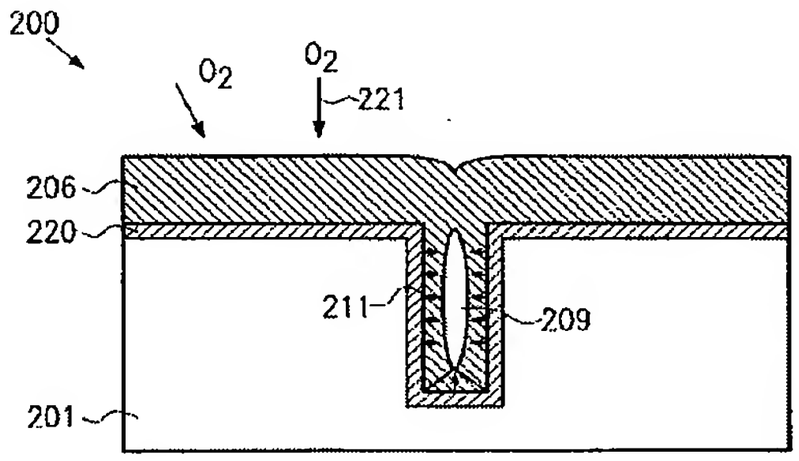


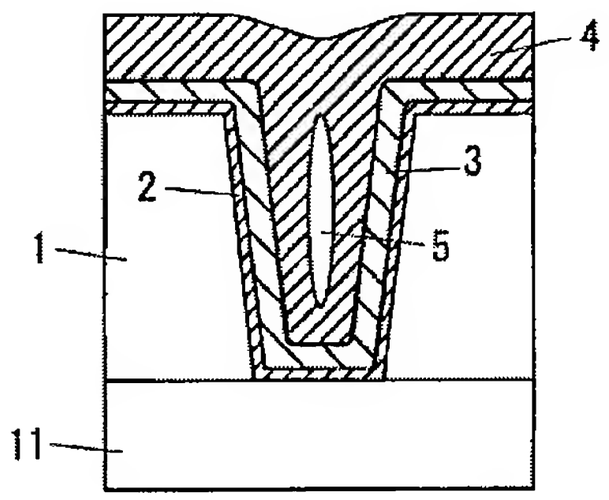
FIG.2c
Wieczorek'696

Wieczorek'696 does not teach, or suggest, (iii) "wherein the expansion layer is made of a silicide" as recited in independent claim 1 as amended, (iv) "wherein the oxidation preventive layer is formed of a silicon nitride film" as recited in claims 5 and 9, (v) "wherein a pressure of the oxidation atmosphere in the expansion step is atmospheric pressure or more" as recited in claims 6 and 10, and (vi) "a method for manufacturing semiconductor device, comprising the steps of: forming a first film, an oxidation preventive layer that prevents permeation of moisture into the element, on a concave and convex portion formed by an element on a semiconductor substrate; forming a second film, an expansion flow layer that can be oxidized, expanded and fluidized by a heat treatment in an oxidation atmosphere and that has an insulating property, on the oxidation preventive layer; and exposing the semiconductor substrate, on which the oxidation preventive layer and the expansion flow layer have been formed, to the heat treatment in an oxidation atmosphere, in order to oxidize, expand and fluidize the expansion flow, thereby eliminating bubbles or open pores generated in the

expansion flow layer, wherein the expansion flow layer fills the concave and convex portion" as recited in claim 7 as amended.

As illustrated in Fig. 2C (see below) of Applicants' disclosure as originally filed (p. 12, lines 20 to p. 14, line 16), a semiconductor device includes a semiconductor substrate (11) having a concave and convex portion (1), and an oxidation preventive layer (2), an expansion layer (3), and an insulting film (4), formed on the concave and convex portion (1) of the substrate (11) in order.

Fig. 2C



Applicants' disclosure

The Examiner contends that Wieczorek'696 teaches all of the elements as claimed in independent claim 1 (Office Action, dated March 10, 2009, p. 2, line 8 to p. 3, line 2). However, the spacer layer (220) in the semiconductor structure (200) of Fig. 2c of Wieczorek'696, an expansion layer alleged by the Examiner, is comprised of silicon (p. 3, paragraph [0033], lines 15-17), not composed of silicide, a material forming the expansion layer (3) as claimed in independent claim 1 as amended. Silicide, contrary to silicone, is a binary compound of silicon with a more electropositive element or group, for example, magnesium silicide (Mg_2Si) (see Exhibit 1, a definition of silicide in Merriam-Webster Online Dictionary and magnesium silicide in ChemIDplus Lite of U.S. National Library of Medicine).

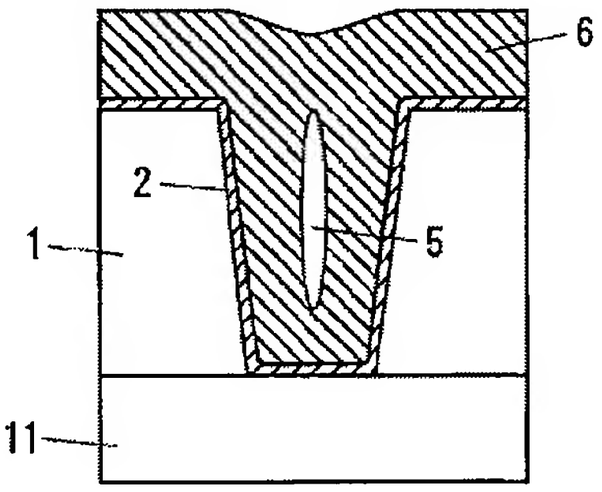
The Examiner contends with respect to claims 5 and 9 that Wieczorek'696 teaches the oxidation preventive layer (not shown) is formed of a silicon nitride film (Office Action, dated March 10, 2009, p. 3, lines 15-16). Wieczorek'696 describes that "the substrate (201) may be comprised of an oxidizable material, a thin non-oxidizable liner (not shown) may be formed prior to depositing the spacer layer (220)" at p. 3, paragraph [0033], lines 10-15, but does not disclose what material may be utilized for forming the thin non-oxidizable liner.

With respect to claims 6 and 10, the Examiner contends that Wieczorek'696 inherently teaches pressure for oxidation is atmospheric pressure because Wieczorek'696 does not mention any thing about using chamber or furnace for enclosing the substrate in controlled atmosphere to oxidize silicon layer (Office Action, dated March 10, 2009, p. 4, lines 1-4). Applicants object to the Examiner's inherency argument. Inherency must be based on an otherwise sufficient disclosure such that the implied subject matter is the natural result flowing from the otherwise sufficient disclosure, and it cannot be based on mere probabilities or possibilities. Continental Can Co. USA v. Monsanto Co., 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991). The Examiner's naked speculation falls far short of establishing that because a pressure for oxidation is not explicitly mentioned in Wieczorek'696, the pressure for oxidation utilized in Wieczorek'696 is inherently atmospheric pressure.

With respect to claim 7, the Examiner contends that Wieczorek'696 teaches all of the elements as claimed in independent claim 7 (Office Action, dated March 10, 2009, p. 3, lines 3-14). During an oxidation process, the semiconductor structure (200) as detailed in Fig. 2c of Wieczorek'696 is exposed to an oxidizing ambient, and subsequently, a stress (211) by the excessive volume produced due to the oxidation of the spacer layer (220) is exerted to the dielectric layer (206), an insulating film alleged by the Examiner, thereby enclosing a void (209) in the dielectric layer (206). Indeed, in the oxidation process of Wieczorek'696, the spacer layer (220) has only an expansion property and the dielectric layer (206) has only a

fluidization property (see Wieczorek'696, p. 4, paragraph [0035]). In contrast, the expansion layer (6), as claimed in independent claim 7 as amended, another embodiment of the present invention (see Fig. 7B below and p. 19, line 12 to p. 20), both expands and is fluidized so that the concave and convex portion (1) is filed with the expansion flow layer.

Fig. 7B



Applicants' disclosure

New independent claim 11 contains "a method for manufacturing semiconductor device, comprising the steps of...wherein the expansion layer is made of aluminum, tantalum or an alloy of aluminum or tantalum" as supported on p. 7, lines 2-5 and the original claim 3 as cancelled of Applicants' disclosure as originally filed. As admitted by the Examiner, Wieczorek'696 does not teach, or suggest, that the expansion layer is made of aluminum, tantalum or an alloy thereof as recited in new claim 11 (Office Action, dated March 10, 2009, p. 5, lines 8-9). Therefore, new claim 11 is independently patentable over Wieczorek'696.

In summary, the Examiner has failed to establish a prima facie case of anticipation against claims 1, 5-7 and 9-11 using the disclosure of Wieczorek'696, because all elements of the claims are not identically disclosed in a single reference. Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick, 221 U.S.P.Q. 481, 485 (Fed. Cir. 1984). Thus, the rejections under §102 should be reconsidered and withdrawn.

b. The Section 103 Rejection

A prima facie case of obviousness requires a showing that the scope and content of the prior art teaches each and every element of the claimed invention, and that the prior art provides some teaching, suggestion or motivation, or other legitimate reason, for combining the references in the manner claimed. KSR International Co. v. Teleflex Inc., 127 S.Ct. 1727, 11739-41 (2007); In re Oetiker, 24 U.S. P.G.2d 1443 (Fed. Cir. 1992).

In this case, the Examiner failed to establish a prima facie case of obviousness against claims 4 over the combination of Wieczorek'696 and admitted prior art, and against claim 8 over combination of Wieczorek'696 and Ishitsuka'646, respectively, because the combination fails to teach all of the limitations of the claims. In addition, the Examiner has failed to establish a prima facie case of obviousness against new independent claim 11 corresponding claim 3 as cancelled, because the combination of Wieczorek'696 and Maniar'176 fails to teach all of the limitations of the claim.

(a). The Section 103 Rejection based on the Combination of Wieczorek'696 and Admitted Prior Art

The combination of Wieczorek'696 and admitted prior art fails to teach a prima facie case of obviousness against claim 4 because of the following reasons.

i. Wieczorek'696

Wieczorek'696 is discussed above.

As admitted by the Examiner (Office Action, dated March 9, 2009, p. 5, lines 1-3), Wieczorek'696 does not teach, or suggest, "wherein the insulating film is a silicon oxide film containing at least one of phosphorus, arsenic, boron, fluorine and a halide" as recited in claim 4.

In addition, Wieczorek'696 does not teach, or suggest, "the method for manufacturing semiconductor device according to claim 1, wherein the insulating film is a silicon oxide film containing at least one of phosphorus, arsenic, boron, fluorine and a halide" as recited in claim 4.

ii. Admitted prior art (JP 5-67607 and JP 10-275805)

Admitted prior art (JP 5-67607 and JP 10-275805) relates to method for manufacturing semiconductor device having a flattened insulating film (p. 3, line 16 to p. 4, line 15 of Applicants' disclosure as originally filed). A semiconductor device of JP 10-275805 includes a silicon nitride film formed on the seminconductor device, an insulating film formed on the silicon nitride film, which is a BPSG film containing boron and phosphorus, and SOG film coated on the insulating film (p. 3, line 16 to p. 4, line 15 of Applicants' disclosure as originally filed).

Admitted prior art does not teach, or suggest, "the method for manufacturing semiconductor device according to claim 1, wherein the insulating film is a silicon oxide film containing at least one of phosphorus, arsenic, boron, fluorine and a halide" as recited in claim 4.

iii. Summary of the Disclosures regarding the Rejection of Claim 4 over the Combination of Wieczorek'696 and Admitted Prior art

The combination of Wieczorek'696 and admitted prior art fails to teach, or suggest, (i) "the method for manufacturing semiconductor device according to claim 1, wherein the insulating film is a silicon oxide film containing at least one of phosphorus, arsenic, boron, fluorine and a halide" as recited in claim 4. In other words, as detailed in Applicants' Argument of Section 102 rejections above, the combination does not teach, or suggest, the

subject matter of independent claim 1 as amended including the expansion layer made of a silicate.

For this reason, no prima facie showing of obviousness has been under against claim 4.

(b). The Section 103 Rejection based on the combination of Wieczorek'696 and Ishitsuka'646

The combination of Wieczorek'696 and Ishitsuka'646 fails to teach a prima facie case of obviousness against claim 8 because of the following reasons.

i. Wieczorek'696

Wieczorek'696 is discussed above.

As admitted by the Examiner (Office Action, dated March 9, 2009, p. 4, lines 12-14), Wieczorek'696 does not teach, or suggest, "wherein the expansion flow layer is made of a polycrystalline silicon or an amorphous silicon containing at least one of boron, phosphorus and fluorine" as recited in claim 8.

In addition, Wieczorek'696 does not teach, or suggest, "the method for manufacturing semiconductor device according to claim 7, wherein the expansion flow layer is made of a polycrystalline silicon or an amorphous silicon containing at least one of boron, phosphorus and fluorine" as recited in claim 8.

ii. Ishitsuka'646

Ishitsuka'646 relates to a semiconductor device having a highly reliable groove isolation structure and a process for producing the same (Ishitsuka'646, column 1, lines 12-14). A semiconductor device having an isolation groove (4) in depicted in Figs. 61-64 of

Ishitsuka'646 (Also see column 29, lines 34-60 of Ishitsuka'646) comprises polycrystalline silicon film (22) deposited on silicon nitride film (3), and silicone oxide film (7) deposited on polycrystalline silicon film (22) to embed silicone oxide film (7) in groove (4a), wherein silicon oxide film (7), and silicon oxide film (23) which polycrystalline silicon film (22) is oxidized to, are removed to leave silicone oxide films (7, 23) only in groove (4a), thereby forming element isolation groove (4).

Ishitsuka'646 does not teach, or suggest, (i) "the method for manufacturing semiconductor device according to claim 7, wherein the expansion flow layer is made of a polycrystalline silicon or an amorphous silicon containing at least one of boron, phosphorus and fluorine" as recited in claim 8.

Ishitsuka'646 only teaches a polycrystalline silicone film (22) which is oxidized to silicon oxide film (23) (Ishitsuka'646, column 29, lines 34-60), not a polycrystalline silicon or an amorphous silicon containing at least one of boron, phosphorus and fluorine as an expansion flow layer as required in claim 8.

iii. Summary of the Disclosures regarding the Rejection of Claim 8 over the Combination of Wieczorek'696 and Ishitsuka'646

The combination of Wieczorek'696 and Ishitsuka'646 fails to teach, or suggest, (i) "the method for manufacturing semiconductor device according to claim 7, wherein the expansion flow layer is made of a polycrystalline silicon or an amorphous silicon containing at least one of boron, phosphorus and fluorine" as recited in claim 8. Indeed, the combination discloses neither the method for manufacturing semiconductor device according to claim 7 comprising an expansion flower layer which by itself can be oxidized, expanded and fluidized, and fill the concave and convex portion nor an expansion layer containing a

material of polycrystalline silicon or an amorphous silicon containing at least one of boron, phosphorus and fluorine as recited in claim 8.

For this reason, no prima facie showing of obviousness has been under against claim 8.

(c). The Section 103 Rejection based on the combination of Wieczorek'696 and Maniar'176

The combination of Wieczorek'696 and Maniar'176 fails to teach a prima facie case of obviousness against new independent claim 11 corresponding claim 3 as cancelled because of the following reasons.

i. Wieczorek'696

Wieczorek'696 is discussed above.

As admitted by the Examiner (Office Action, dated March 9, 2009, p. 5, lines 8-9), Wieczorek'696 does not teach, or suggest, (i) "wherein the expansion layer is made of aluminum, tantalum or an alloy of aluminum or tantalum" as recited in new independent claim 11 corresponding to claim 3 as cancelled.

ii. Maniar'176

Maniar'176 relates to methods for providing trench isolation in semiconductor devices (Maniar'176, column 1, lines 23-25). As illustrated in Fig. 4 of Maniar'176, a semiconductor device (10) comprises a trench isolating material (30) deposited over a substrate (12), thereby filling trench (22). In Maniar'176, insulating materials such as aluminum oxide and titanium oxide are utilized as suitable isolating materials (Maniar'176, column 4, lines 26-43).

Maniar'176 does not teach, or suggest, (i) "a method for manufacturing semiconductor device, comprising the steps of:... forming a second film, an expansion layer that can be oxidized and expanded by a heat treatment in an oxidation atmosphere, on the oxidation preventive layer;...and exposing the semiconductor substrate, on which the oxidation preventive layer, the expansion layer and the insulating film have been formed, to the heat treatment in an oxidation atmosphere, in order to fluidize the insulating film and to oxidize and expand the expansion layer, thereby eliminating bubbles generated in the insulating film, wherein the expansion layer is made of aluminum, tantalum or an alloy of aluminum or tantalum" as recited in new claim 11.

Maniar'176 only teaches an insulating layer made of aluminum oxide (Maniar'176, column 4, lines 26-43). Maniar'176 discloses neither an expansion layer which can expand and thus eliminate bubbles in the insulting layer nor an expansion layer made of aluminum, tantalum or an alloy thereof as required in new claim 11.

iii. Summary of the Disclosures regarding the Rejection of Claim 11 over the Combination of Wieczorek'696 and Maniar'176

The combination of Wieczorek'696 and Maniar'176 fails to teach, or suggest, (i) "a method for manufacturing semiconductor device, comprising the steps of: forming a first film, an oxidation preventive layer that prevents permeation of moisture into the element, on a concave and convex portion formed by an element on a semiconductor substrate; forming a second film, an expansion layer that can be oxidized and expanded by a heat treatment in an oxidation atmosphere, on the oxidation preventive layer; forming a third film, an insulating film that can be fluidized by the heat treatment in the oxidation atmosphere, on the expansion layer; and exposing the semiconductor substrate, on which the oxidation preventive layer, the expansion layer and the insulating film have been formed, to the heat treatment in an

oxidation atmosphere, in order to fluidize the insulating film and to oxidize and expand the expansion layer, thereby eliminating bubbles generated in the insulating film, wherein the expansion layer is made of aluminum, tantalum or an alloy of aluminum or tantalum" as recited in new independent claim 11.

For this reason, no prima facie showing of obviousness has been under against new claim 11.

III. CONCLUSION

The Examiner has failed to establish a prima facie case of anticipation under 35 U.S.C. § 102(a) based on Wieczorek'696, or of obviousness under 35 U.S.C. § 103(a) based on the combination of Wieczorek'696 and admitted prior art, Wieczorek'696 and Ishitsuka'646, and Wieczorek'696 and Maniar'176 because: (i) Wieczorek'696 fails to teach each and every limitation of claims 1, 5-7 and 9-11; and (ii) the combination of Wieczorek'696 and admitted prior art, Wieczorek'696 and Ishitsuka'646, and Wieczorek'696 and Maniar'176, does not teach all the limitations of claims 4, 8 and 11, respectively.

For all of the above reasons, claims 1 and 4-11 are in condition for allowance, and a prompt notice of allowance is earnestly solicited.

The below-signed attorney for Applicant welcomes any questions.

Respectfully submitted,

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